Design Verification Engineer (PCIe, CXL, UVM, System Verilog)
Design & Verification Engineer

PLDA part of Rambus, a premier chip, and silicon IP provider, is seeking to hire an exceptional mid-level Design and Verification Engineer to join our PHY integration team in Sofia, Bulgaria.
The successful candidate will participate in pre-silicon RTL Design and Verification activities related to PCIe Controller Soft IP development and PHYs integrations, on leading-edge PCI-Express and CXL controller technologies. This is a Full Time position.

Rambus offers a flexible work environment, embracing a hybrid approach for the majority of our office-based roles.
We encourage employees to spend an average of at least three days per week working onsite while also allowing for two days of remote work if you are located in Sofia.

Your main responsibilities will be:

* Verilog RTL design in order to integrate different IPs together such as PCIe IP with vendor PHY module
* Verifying the IP integration with dedicated simulation environment
* Development and support test cases of different verification environments
* Support worldwide customers on the IP integration
* Get familiar to existing verification process, propose improvements
* Maintain the traceability from the customer specification or the product specification to the architecture and verification results.
* Track and maintain verification productivity metrics
* Reporting periodically on progress and difficulties

Your Qualifications:

Positive and self-driven achiever with:

* "Can Do" Attitude
* Bachelor or Master's degree in Electronics Engineering, Computer Science, or related disciplines
* Strong analytical and problem-solving skills
* Excellent interpersonal skills
* Open for traveling abroad
* Work in international organization and specially with teams in France, USA, Taiwan and India
* Because Rambus operates internationally, very good English is important for the position

Your technical experience:

* 6+ years experience verification with Verilog, SystemVerilog, FPGA prototyping
* 6+ years experience with complex ASIC/VLSI verification
* 6+ years experience with Avery or UVM. Any 3rd party VIP experience is a plus.
* 6+ years experience in multinational company
* Experience with creating documentation, python, shell & etc.

We will offer you:
* Participation in unique projects for Bulgarian hi-tech industry
* Gaining strong and valuable engineering experience, opportunity to fulfill an exciting career.
* An opportunity to be a part of a proud and motivated team, be in a company which inspires performance, achievements, creativity

Benefits:
* Attractive salary
* 25 days paid leave
* Food vouchers
* Additional bonus
* Hybrid or fully remote if you are outside of Sofia
* Additional health care
* Multisport card
* Public transport card (if you are in Sofia)
* option for office parking space
* 2 times per week free lunch at the office

If you are interested, please sent your CV in English.
We will be happy to invite you to an interview!

Contact:

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